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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/628,049	07/27/2000	Thomas H. Distefano	THESSERA 3.0-102 II DIV	2892

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EXAMINER
GRAYBILL, DAVID E

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/628,049	DISTEFANO, THOMAS H.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2002* .

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features specified in claims 5-8 must be shown or the feature canceled from the claim. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani (5473512).

At column 3, line 39 to column 4, line 22; column 4, lines 52-67; column 5, line 42 to column 6, line 14; column 6, lines 41-44; and column 7, last line to column 8, line 23, Degani teaches the following:

1. A method of making a semiconductor chip assembly comprising the steps of: (a) providing a dielectric element 200 having top and bottom surfaces and terminals 223 on said bottom surface; (b) supporting semiconductor chip 300 having a front surface with contacts 301, 302 thereon, a rear surface and edges extending between said front and rear surfaces above said top surface of said dielectric element by means of a plurality of posts 253, 254 extending between said rear surface of the chip and the top surface of the dielectric element; then (c) applying a first curable encapsulant 304 so that said first encapsulant penetrates between said rear surface and said top surface and penetrates between said posts; then (d) curing said first encapsulant to form a flexible rear encapsulant; (e) connecting said contacts to said terminals by connecting flexible leads 311, 312 between said contacts on said front surface and electrically conductive elements 262, 266 on said dielectric element; and (f) providing a flexible lead encapsulant 400 around said chip and said flexible leads.

2. A method as in 1 wherein said step of providing a flexible lead encapsulant includes the steps of applying a second liquid of different composition from said first encapsulant and curing said second liquid.

3. A method as in 2 wherein said step of applying said second liquid is performed after said step of curing said first liquid encapsulant.

5. A method as in 1 wherein said step of applying said first liquid includes the steps of placing said first liquid on said top surface of said dielectric element at edges of said chip and applying a gas ["air"] under pressure [atmospheric] around the chip and dielectric element to thereby force said first liquid into the spaces between said posts.

6. A method as in 5 wherein said gas pressure is maintained during said step of curing said first liquid.

To further clarify the teaching of a flexible rear encapsulant, all materials are capable of being flexed; hence, flexibility is an inherent property of the rear encapsulant.

However, Degani does not appear to explicitly teach a first liquid. Nonetheless, Degani teaches that the first encapsulant is an epoxy that has been cured by heating, and official notice is taken that it is well known to provide as a liquid an epoxy cured by heating. Moreover, it would have been obvious to use the well known epoxy as the epoxy of Degani because it would provide an epoxy that is cured by heating.

Claims 4, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani (5473512).

As cited supra Degani teaches the following:

4. A method of making a semiconductor chip assembly comprising the steps of: (a) providing a dielectric element having top and bottom surfaces and terminals on said bottom surface; (b) supporting a semiconductor chip having a front surface with contacts thereon, a rear surface and edges extending between said front and rear surfaces above said top surface of said dielectric element by means of a plurality of posts extending between said rear surface of the chip and the top surface of the dielectric element; then (c) connecting said contacts to said terminals by connecting flexible leads between said contacts and electrically conductive elements on said dielectric element; and (d) applying a first curable liquid 400 so that said first liquid penetrates between said rear surface and said top surface and penetrates between said posts, and so that said first liquid surrounds said flexible leads; then (e) curing said liquid to form a flexible rear encapsulant between the rear surface of the chip and the dielectric element and to form a flexible lead encapsulant integral with said rear around said chip and said flexible leads.

7. A method as in 4 wherein said step of applying said first liquid includes the steps of placing said first liquid on said top surface of said dielectric element at edges of said chip and applying a gas under pressure around the chip and dielectric

element to thereby force said first liquid into the spaces between said posts.

8. A method as in 7 wherein said gas pressure is maintained during said step of curing said first liquid.

Claims 9-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ishida (5289039) and Burns (5369056).

At column 4, lines 22-42, column 5, lines 17-20 and 45-52, column 6, lines 18-22 and 32-45, and column 7, lines 3-6, Ishida teaches the following:

9. A method of enhancing the reliability of electrical connections in a semiconductor package during operation of the chip, comprising the steps of: (a) providing a semiconductor chip 1 having a front surface and a rear surface, said front surface having contacts [inherent]; (b) providing flexible leads 3 extending from said contacts on said front surface of said chip by wire bonding, said flexible leads being connected to said contacts at joints on said front surface; (c) placing a spreader 7 above said front surface, said spreader inherently having a coefficient of thermal expansion; and (d) disposing a liquid encapsulant 6 between said front surface and said spreader and around said leads and curing said encapsulant, whereby the motion of the leads during thermal cycling is inherently constrained.

10. The method as in 9, further comprising the step of providing a predetermined geometry for the cured encapsulant so as to inherently affect the constraint of the leads.

11. A method as in 9 wherein said steps of placing said spreader and disposing and curing said encapsulant are performed so that the cured encapsulant has edges intersecting said spreader and extending downwardly away from said spreader and said spreader extends outwardly beyond intersections of said edges and said spreader.

13. A method as in 9 wherein said step of providing said flexible leads by wire bonding includes forming bonding wire so that said bonding wire includes loops projecting upwardly away from said front surface and away from said joints.

14. A method as in 13 wherein said step of forming bonding wire includes forming downwardly-projecting portions extending from said loops downwardly beyond the front surface of the chip.

15. A method of making a semiconductor package comprising the steps of; (a) positioning a semiconductor chip having a front surface with contacts thereon and having a rear surface and an element 2 having conductive features thereon 20 so that said element extends beneath said rear surface of said chip and said front surface of said chip faces upwardly away from said element; (b) providing flexible leads extending from said

contacts on said front surface of said chip and extending downwardly to said element, said flexible leads being connected to said contacts at joints on said front surface; (c) placing a spreader above said front surface, said spreader having a coefficient of thermal expansion; and (d) disposing a liquid encapsulant between said front surface and said spreader and around said leads and curing said encapsulant, whereby the motion of the leads during thermal cycling is constrained.

16. A method as in 15 wherein said step of providing said flexible leads is performed by wire bonding.

17. A method as in 16 wherein said step of wire bonding includes forming bonding wire into loops projecting upwardly from said front surface and downwardly-projecting portions extending downwardly from said loops to said element.

However, Ishida does not appear to explicitly teach the spreader having a coefficient of thermal expansion substantially equal to the coefficient of thermal expansion of the chip.

Regardless, at column 3, lines 21-26 Burns teaches this process. In addition, it would have been obvious to combine the process of Burns with the process of Ishida because it would prevent warping.

Also, Ishida does not appear to explicitly teach the following:

12. A method as in 11 wherein said steps of placing said spreader and disposing and curing said encapsulant are performed so that said edges of said cured encapsulant include opposite edges sloping outwardly away from one another in the downward direction away from said spreader.

Nevertheless, at column 7, lines 17-25, Burns teaches edges of a cured encapsulant include opposite edges sloping outwardly away from one another in a downward direction away from a top surface. Furthermore, it would have been obvious to combine the process of Burns with the process of Ishida because it would facilitate removal of the encapsulant from the mold.

Applicant's remarks filed ?? have been fully considered and are adequately addressed in the rejection supra.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
26-Aug-02